

# 14 pin Dual-in-Line

# 60.0MHz to 240.0MHz

- Frequency range 60MHz to 240MHz
- **LVPECL Output**
- **Supply Voltage 3.3 VDC**
- Phase jitter 0.2ps typical
- Pull range from ±30ppm to ±150ppm

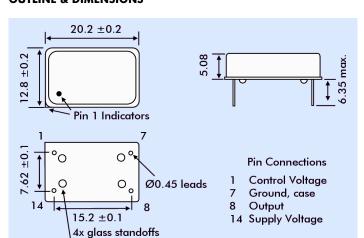
### **DESCRIPTION**

GPA14 VCXOs are packaged in a 14 pin dual-in-line package. Typical phase jitter for GPA series VCXOs is 0.2 ps. Output is LVPECL. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

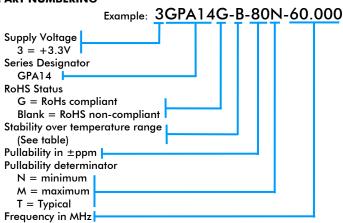
SPECIFICATION		
Frequency Range:	60.0MHz to 240.0MHz	
Supply Voltage:	3.3 VDC ±5%	
Output Logic:	LVPECL	
RMS Period Jitter		
60.0MHz ~ 120MHz:	2.5ps typical	
120MHz ~ 240MHz:	4.7ps typical	
Peak to Peak Jitter		
60.0MHz ~ 120MHz:	17.5ps typical	
120MHz ~ 240MHz:	24.5ps typical	
Phase Jitter:	0.2ps typical	
Initial Frequency Accuracy:	Tune to the nominal frequency	
	with Vc= 1.65 ±0.2VDC	
Output Voltage HIGH (1):	Vdd-1.025V minimum	
	Vdd-0.880V maximum	
Output Voltage LOW (0):	Vdd-1.810V minimum	
	Vdd-1.620V maximum	
	(RL=50 \( \Omega \) to Vdd-2V)	
Pulling Range:	From ±30ppm to ±150ppm	
Control Voltage Range:	1.65 ±0.35 Volts	
Temperature Stability:	See table	
Output Load:	50Ω into Vdd or Thevenin equiv.	
Rise/Fall Times:	0.5ns typ., 0.7ns max.	
	20% Vdd to 80% Vdd	
Duty Cycle:	50% ±5%	
Class Time	(Measured at Vdd-1.3V)	
Start-up Time:	10ms maximum, 5ms typical	
Current Consumption:	75mA maximum at 212.5MHz	
Ctatia Disabanas Bastastian	80mA maximum at 622.08MHz 2kV maximum	
Static Discharge Protection:		
Storage Temperature: Ageing:	-55° to +150°C	
Enable/Disable:	±2ppm per year maximum  Not implemented - 4 pin package	
RoHS Status:	Fully compliant or non-compliant	
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# **OUTLINE & DIMENSIONS**



## **PART NUMBERING**



## FREQUENCY STABILITY

<b>Stability Code</b>	Stability ±ppm	Temp. Range
Α	25	0°∼+70°C
В	50	0°∼+70°C
С	100	0°∼+70°C
D	25	-40°~+85°C
E	50	-40°∼+85°C
F	100	-40°∼+85°C

If non-standard frequency stability is required Use 'I' followed by stability, i.e. I20 for ±20ppm